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TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

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U S APPLICATION NO. (If known, see 37 CFR 1 5)	
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INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE00/02875	23 August 2000	25 August 1999

TITLE OF INVENTION
Treiberschaltung und Verfahren zum Betreiben einer Treiberschaltung

APPLICANT(S) FOR DO/EO/US
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Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [X] This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. [ ] The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [X] is attached hereto (required only if not communicated by the International Bureau).
   b. [ ] has been communicated by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [ ] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. [ ] is attached hereto.
   b [ ] has been previously submitted under 35 U.S.C 154(d)(4).
7. [ ] Amendments to the claims of the International Aplication under PCT Article 19 (35 U.S.C 371(c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. [ ] An oath or declaration of the inventor(s) (35 U.S C. 371(c)(4)).
10. [ ] An English lanugage translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [ ] A FIRST preliminary amendment.
14. [ ] A SECOND or SUBSEQUENT preliminary amendment.
15. [ ] A substitute specification.
16. [ ] A change of power of attorney and/or address letter.
17. [ ] A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1 821 - 1 825.
18. [ ] A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. [ ] A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. [ ] Other items or information:

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I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1 10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington D.C 20231

Mary A. Florin
(Typed or printed name of person mailing paper or fee)

Mary A. Florin
(Signature of person mailing paper or fee)

U.S. APPLICATION NO (If known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
N/A 10/069806	PCT/DE00/02875	32226.18

21. ☒ The following fees are submitted:	CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1 445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1040.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$890.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$740.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$710.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**		
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Surcharge of **$130.00** for furnishing the oath or declaration later than ☒ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1 492(e)).	$ 130.00	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	17 - 20 =	0	x $18.00	$ 0	
Independent claims	0 - 3 =	0	x $84.00	$ 0	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $280.00	$ 0	
TOTAL OF ABOVE CALCULATIONS =				$1,020	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2 +				$	
SUBTOTAL =				$1,020	
Processing fee of **$130.00** for furnishing the English translation later than ☒ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				$ 130.00	
TOTAL NATIONAL FEE =				$1,150	
Fee for recording the enclosed assignment (37 CFR 1 21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$ 0	
TOTAL FEES ENCLOSED =				$1,150	
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a. ☒ A check in the amount of $ 1,150 to cover the above fees is enclosed.

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d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO·

SIGNATURE

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47,976
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Description

Driver circuit and method for operating a driver circuit

The present invention generally relates to a driver circuit and a method for operating such a driver circuit.

Driver circuits are used in diverse ways in integrated digital circuitry, for example as drivers for lines, busses of integrated circuits or the like.

In recent years, the requirements imposed on electronic components and thus also on the driver circuits, in particular in electronic systems clocked at high speed, have risen rapidly. One of these requirements that have risen relates for example to electromagnetic compatibility (EMC).

Integrated digital circuits are generally connected via conductive connections to peripheral devices, power sources and the like. This results, inter alia, in parasitic capacitances which lead to disadvantageous signal alterations. External loads, the parasitic capacitances and also the driver transistors themselves form an electronic network in which resonance effects, reflections and the like can occur. These generate transient signals which can deviate from their envisaged magnitude and shape and exceed or fall below their final voltage states. On account of the densely packed design on chips, such transient signals can adversely affect not only their own signal lines themselves but also signal lines of adjacent electronic components.

On account of the increasing requirements, there is a

need to improve electronic components, corresponding driver circuits and the like, in such a way that these disadvantages can be avoided.

US-A-5,537,067 describes, for example, a driver circuit which can be operated in order to regulate the rise times and fall times of signals supplied to a load. This driver circuit has a first inverter with a PMOS transistor and an NMOS transistor and a resistor. A second inverter has a PMOS transistor and an NMOS transistor. The resistor and additionally provided capacitors increase the transition times of the output driver signal in order to control the electromagnetic radiation caused by short transition times of the output signal.

It is an object of the present invention to provide an improved driver circuit and an improved method for operating a driver circuit with which, in particular, the electromagnetic compatibility of electronic components can be improved.

This object is achieved, in accordance with the first aspect of the invention, by means of a driver circuit in accordance with the independent patent claim 1. Advantageous developments of the driver circuit according to the invention emerge from the subclaims.

The invention provides a driver circuit, having at least one input node for an input signal and at least one output node for an output signal, having one or more, preferably two, sub-drivers and having a feedback circuit, which has one or more evaluation circuits and one or more feedback capacitors, the evaluation circuit(s) being connected to the sub-driver(s) and the feedback capacitor(s) respectively being provided between an output node of the driver circuit and an input node of an evaluation circuit.

Such a driver circuit enables the electromagnetic compatibility of electronic components, in particular of integrated circuits, to be greatly improved.

The basic concept of the driver circuit according to the invention is that firstly a signal with the least harmonics possible can be generated, which signal is supplied to a load. By way of example, the signal may be a current which can be supplied for example as charging/discharging current to a load capacitance during the switching edges. Since the interference spectrum of a driver circuit depends on the temporal profile of the current which charges the load capacitance, in particular a $\sin^2$-shaped current, which has a favorable interference spectrum, is advantageous as low-harmonics current. The low-harmonics current is preferably generated in the at least one sub-driver. This will be explained in more detail in the further course of the description.

Usually, the rise times and fall times of a driver circuit - and thus also the temporal current profile - depend on the magnitude of the load or the load capacitance. In the case of small loads, in particular, a large interference potential is present, since an unregulated driver then reverses the charge of said loads too quickly.

Therefore, the intention is that the driver circuit can additionally set an edge steepness of the signal (output signal coupled out from the driver circuit) supplied to the load, which edge steepness is independent of the present load situation. The load-independent edge steepness is set by means of the feedback circuit, in which a present edge steepness is in each case measured and evaluated. On the basis of the evaluation results, it is possible to adapt the driver strength in the at least one sub-driver in real

time. However, it is also possible for the driver strength to be adapted progressively or the like.

The present edge steepness of the output signal is measured by means of the at least one feedback capacitor. Here a displacement current is generated, which is coupled into the at least one evaluation circuit and evaluated there. The evaluation can be effected for example in such a way that the measured displacement current is compared with corresponding reference current values. Afterward, the evaluated results are forwarded as control signals to the at least one sub-driver, where the driver strength thereof can be correspondingly adapted or readjusted. What is achieved in this way is that the same displacement current always occurs in the feedback capacitor. Examples of the construction and the method of operation of the feedback circuit will be explained in more detail in the further course of the description.

The driver circuit according to the invention thus makes it possible to be able to measure the output characteristic of the driver circuit directly, to evaluate the measurement results and to be able to bring about an alteration and adaptation of the driver strength in a manner dependent on the evaluated results. This makes it possible to achieve rise times and fall times that are largely independent of the output load. This means, in particular, that even temporary interference, such as, for example, the in-antiphase switching of adjacent, capacitively coupled lines or the like, does not influence the edge steepness.

The driver circuit according to the invention does not require the magnitude of the load that is connected downstream to be known. All that is important is that the load is smaller than a maximum permissible load.

The driver circuit enables an input signal, for example a binary input signal, to be coupled into it via the at least one input node, the signal being converted in the driver circuit and being output to a load, for example a load capacitance, via the at least one output node.

The driver circuit has at least one sub-drive, which may be designed as a so-called pull-up driver (a driver for the positive edge) and/or as a pull-down driver (a driver for the negative edge).

The construction of a driver circuit according to the invention will now firstly be described below. However, it goes without saying here that the invention is not restricted to the examples mentioned.

The driver circuit may have one or more sub-drivers. The driver circuit may advantageously have two sub-drivers which may be designed for example as pull-up driver and as pull-down driver.

The at least one sub-driver is connected to at least one output node, which is likewise connected to a load. Via the output node, the at least one sub-driver is also connected to the at least one evaluation circuit of the feedback device. At least one feedback capacitor is provided in this connecting line.

Preferably, the at least one input node for the input signal may be connected to the at least one sub-driver. A signal can be coupled into the at least one sub-driver via this connection, on the basis of which signal it is possible to determine in the sub-driver whether the latter must be activated. The value for the magnitude of the value to be readjusted or changed for the driver strength is coupled into the sub-driver(s) via the connection between sub-driver and evaluation circuit.

Furthermore, the at least one input node for the input signal may be connected to the at least one evaluation circuit. Via this connection, it is possible, for example, for the feedback circuit to be temporarily shut down if no transients are to be expected. This leads to a reduction in the power loss.

In a further configuration, two or more sub-drivers and two or more evaluation circuits may be provided, each sub-driver being connected to an evaluation circuit.

In such a configuration, it is advantageous likewise for two or more feedback capacitors to be provided, each feedback capacitor being provided between an output node of the driver circuit and an input node of an evaluation circuit.

The at least one output node may advantageously be connected or be able to be connected to a load capacitance. The load capacitance may be, on the one hand, the capacitance of a load connected to the driver circuit, for example an electronic component. Furthermore, the term load capacitance may also encompass parasitic capacitances or the like which occur at the output of the driver circuit or in the connection of the driver circuit to the respective load.

The input node or nodes of the evaluation circuit(s) are preferably of low-impedance design. This ensures that, during a transient, a small displacement current can flow via the feedback capacitor, which is then coupled into the evaluation device. Said displacement current is measured and evaluated by the feedback circuit.

The at least one sub-driver may preferably have one or more transistors. In the simplest case, the sub-driver

may have a single transistor. However, more complex configurations are also conceivable, so that the invention is not restricted to a specific number of transistors.

One of the transistors may be designed, for example, as the actual driver transistor. Furthermore, an additional transistor operating as current source may be provided. Another additional transistor functioning as switch may be provided, as required.

If the driver circuit has two sub-drivers which are designed in the manner mentioned above, it is possible to generate an essentially low-harmonics, in particular $\sin^2$-shaped current. This is done by way of the selection of a suitable dimensioning of the actual driver transistors and of the transistors functioning as current source. The embodiment of some of the transistors as current sources (pre-driver transistors) and the deliberate utilization of the parasitic gate-drain capacitances of the actual driver transistors enables the load current profile to be shaped within wide limits.

Preferably, in each case at least one control transistor may be provided in the at least one sub-driver, said transistor being respectively connected to an evaluation circuit. The signal which is measured by the feedback capacitor and evaluated in the evaluation circuit is coupled out as output signal from the evaluation circuit and serves for actuating the control transistor or transistors, which correspondingly alter(s), for example reduce(s), the strength of the transistor or transistors functioning as pre-driver.

In a further configuration, the at least one evaluation circuit may be designed as an amplifier circuit with one or more transistors. In the amplifier circuit, the

displacement current coupled in via the input node is amplified in such a way that it can be used for actuating the at least one sub-driver, in particular the control transistor provided in the sub-driver. The amplifier comprises one or more transistors, the number of transistors being variable depending on the application and amplifier power.

The at least one feedback capacitor may advantageously be designed as a linear capacitor. However, it is also possible for the at least one feedback capacitor to be designed as a nonlinear capacitor.

In an advantageous configuration, the nonlinear capacitor is formed from at least one PMOS transistor and/or at least one NMOS transistor. In such a configuration, the capacitor may consist of, for example, in each case an NMOS transistor and a PMOS transistor, the two transistors being connected in parallel. However, other configurations are also conceivable, so that the invention is not restricted to the example described.

A nonlinear capacitor constructed from NMOS and PMOS transistors has a voltage-dependent capacitance, so that three voltage-dependent capacitance values can be realized given a corresponding choice of the lengths and widths Wp, Lp, Wn, Ln of the transistors. As a result, the output characteristic curve of the driver circuit can additionally be shaped in a targeted manner. In the evaluation circuit, the displacement current of the feedback capacitor is compared with a reference current. On the basis of the evaluation, the driver strength is set by means of a control signal, so that the same displacement current always occurs in the feedback capacitor. Accordingly, in the case of a nonlinear capacitor, the edge steepness is reduced for high capacitance values and increased for small

capacitance values. What can thus be achieved is that, in a load capacitance, firstly a small current flows, then a larger current and then a smaller current again.

In accordance with the second aspect of the invention, a method for operating a driver circuit according to the invention as described above is provided, which, according to the invention, is characterized in that a low-harmonics current is generated in the driver circuit and supplied to a load, and in that an edge steepness that is independent of the present load situation is set in the driver circuit.

What is achieved by the method according to the invention is that the load is supplied, on the one hand, with a current or a signal with advantageous properties in respect of EMC. On the other hand, an edge steepness that is independent of the present load situation is also achieved, which significantly improves the EMC especially with a small load. With regard to the advantages, actions, effects and mode of operation of the method according to the invention, the above explanations concerning the driver circuit according to the invention are hereby likewise incorporated by reference in their entirety.

Preferred embodiments of the method emerge from the subclaims.

A $\sin^2$-shaped current may advantageously be supplied to the load.

In order to set the load-independent edge steepness, the output characteristic of the driver circuit may preferably be measured by the feedback circuit and evaluated therein, the driver strength of the at least one sub-driver being regulated on the basis of the evaluation results.

In this case, the present edge steepness may be measured by the at least one feedback capacitor and the measured value may be coupled into the at least one evaluation circuit and evaluated. In the evaluation circuit, an output signal is then generated which controls at least one control transistor provided for regulating the driver strength in the at least one sub-driver.

In a particularly advantageous use, the driver circuit according to the invention and/or the method according to the invention may be used for improving the electromagnetic compatibility of electronic components, in particular of integrated circuits.

The invention will now be explained in more detail using exemplary embodiments with reference to the accompanying drawing, in which

Figure 1 shows a schematic view of a first embodiment of the driver circuit according to the invention;

Figure 2 shows a schematic view of a second embodiment of the driver circuit according to the invention;

Figure 3 shows a circuit diagram of the driver circuit in accordance with figure 1;

Figure 4 shows an equivalent circuit diagram of a feedback capacitor;

Figure 5 shows a diagram illustrating the capacitance profile of the feedback capacitor in accordance with figure 4 as a function of the applied voltage;

Figure 6 shows a diagram illustrating the voltage profile of a driver circuit with feedback circuit in the case of a high and a small load; and

Figure 7 shows a diagram illustrating the voltage profile of a driver circuit without a feedback circuit in the case of a high and a small load.

Firstly, figures 1 and 2 illustrate two different embodiments of a driver circuit 10 according to the invention in a general configuration, while figure 3 illustrates a detailed circuit diagram of a driver circuit 10 in accordance with figure 1, in which the individual components are designed in a specified manner.

The driver circuit 10 is used in digital CMOS circuitry for lines, busses or the like.

The driver circuit 10 in accordance with figure 1 has an input node 11, into which an input signal 13, for example a binary signal, is coupled. In the driver circuit 10, the input signal 13 is converted and coupled out as output signal 14 via an output node 12 and is made available to a load, a load capacitance 15 in the present case.

The driver circuit 10 has two sub-drivers 20, 30, namely a pull-up driver 20 and a pull-down driver 30. The two sub-drivers 20, 30 are connected to the input node 11.

Furthermore, a feedback circuit 40 is provided, which constitutes an evaluation circuit 50 and a feedback capacitor 41.

As revealed by figure 4, the feedback capacitor 41 is designed as a nonlinear capacitor having a PMOS transistor 43 and an NMOS transistor 44 connected in parallel therewith. However, the feedback capacitor 41 may also be designed as a linear capacitor or as a nonlinear capacitor with a different configuration. The feedback capacitor 41 is connected to an input node 51 of the evaluation circuit 50 and the output node 12 of the driver circuit 10.

Figure 5 illustrates the qualitative capacitance profile 45 of the feedback capacitor 41 in the design in accordance with figure 4. In this case, it is assumed that the input node 51 is at approximately half the operating voltage potential (Vdd/2). In the regions 46, 47 of higher capacitance, in each case one of the transistors 43, 44 is in inversion. In the present exemplary embodiment, the PMOS transistor 43 is in inversion in the region 46 of the capacitance profile 45, while the NMOS transistor 44 is in inversion in the region 47. In the central region 48 of the capacitance profile 45, the capacitor voltage lies below the respective threshold voltages Vtn and Vtp of the transistors 43, 44, so that only overlap capacitances contribute to the total capacitance.

The input node 51 of the evaluation circuit 50 is designed as a low-impedance node and is at a fixed potential in the present case. The evaluation circuit 50, designed as an amplifier circuit, is furthermore connected to the sub-drivers 20, 30 and the input node 11 for the input signal 13.

Figure 3 illustrates a detailed circuit diagram of the driver circuit 10 in accordance with figure 1. In this case, the individual transistors have been dimensioned in a specific manner, in order to enable a subsequent simulation, the results of which are illustrated in

figures 6 and 7.

As can be seen from figure 3, the evaluation circuit designed as an amplifier circuit consists of a series of transistors 52 to 57, by means of which the desired gain factor is set. The two sub-drivers 20, 30 are each constructed identically and each have a transistor 22, 32 which operates as current source and functions as a so-called pre-driver. Furthermore, an actual driver transistor 21, 31 is provided in each case. The transistors 21, 31 have a large width in order to be able to realize the driver strength. Furthermore, the two sub-drivers 20, 30 are provided with a switch formed by a transistor 23, 33. Finally, another two transistors 24, 34 are provided, which have the function of control transistors. The control transistors 24, 34 are connected to the amplifier circuit 50.

The method of operation of the driver circuit 10 will now be described below.

The great improvement in the electromagnetic compatibility (EMC) of integrated circuits can be achieved if the driver circuit 10 for pads, busses or the like supplies a charging/discharging current to the load capacitance 15 during the switching edges, which current has the least harmonics possible and is, in particular $\sin^2$-shaped. Furthermore, the driver circuit 10 is intended to have an edge steepness that is independent of the present load situation, in order to further improve the EMC especially for small loads

The driver circuit 10 illustrated in figures 1 and 3 unites the property of supplying a $\sin^2$-shaped current with an edge steepness that is independent of the present load 15.

In order to obtain the $\sin^2$-shaped current, the two transistors 22, 32 operate as current sources. The embodiment of the pre-driver transistors 22, 32 as current sources and the targeted utilization of the parasitic gate-drain capacitance of the driver transistors 21, 31 enables the charging current profile to be shaped favorably in respect of EMC ($\sin^2$-shaped).

The load independence is achieved by measuring the edge steepness and correspondingly adapting the driver strength in real time or progressively. For the measurement, use is made of the feedback capacitor 41 connected between the output node 12 of the driver circuit 10 and the input node 51 of the amplifier circuit 50. Since the input node 51 is designed as a low-impedance node, a small current is coupled into the amplifier circuit 50 by the feedback capacitor 41 and is correspondingly evaluated in said amplifier circuit. The output signal of the amplifier circuit 50 serves for actuating the control transistors 24, 34, which suitably readjust, for example reduce, the strength of the pre-driver transistors 22, 32.

In particular, the use of a nonlinear feedback capacitance 41 makes it possible to perform targeted shaping of the edges of the output characteristic curve of the driver circuit. The displacement current supplied by the feedback capacitor 41 is compared with a reference current in the amplifier circuit 50. This evaluation is used to set the driver strength in the two sub-drivers 20, 30 in such a way that the same displacement current always occurs in the feedback capacitor 41. The current profile thus realized has a very favorable interference behavior from an EMC standpoint.

Consequently, the basic concept of the driver circuit 10 according to the invention is that the output

characteristic of the driver circuit 10 can be directly measured and evaluated, and that the driver strength can thereby be adapted correspondingly. As a result, rise/fall times that are largely independent of the output load 15 are achieved. This means, in particular, that even temporary interference, such as, for example, the in-antiphase switching of adjacent, capacitively coupled lines or the like, does not influence the edge steepness.

The possibility of achieving largely load-independent rise and fall times with the driver circuit 10 according to the invention is illustrated with regard to figures 6 and 7. The two figures 6 and 7 in each case show voltage profiles over time which were simulated in a driver circuit 10 specified in accordance with figure 3.

Figure 6 shows the voltage profiles for different loads for a driver circuit 10 in accordance with the present invention which is provided with a feedback circuit 40. Curve 70 shows the voltage profile for a large load capacitance of 50 pF. As revealed by the illustration, the voltage profile has rise edges 71 and fall edges 72, the rise time being approximately 10 ns. The fall time is approximately the same length. In this exemplary embodiment, rise time is understood to be that period of time which is required by a voltage signal in order to pass from 10% of the operating voltage (0.25 V) to 90% of the operating voltage (2.25 V). Conversely, fall time is understood to be that period of time which is required by a voltage signal in order to pass from 90% of the operating voltage to 10% of the operating voltage.

Curve 73 shows the voltage profile for a small load capacitance of 5 pF. As can be seen from figure 6, the voltage profile has rise edges 74 and fall edges 75,

the rise time and the fall time being approximately 8 ns.

Figure 6 thus makes it clear that essentially load-independent voltage profiles can be achieved by using the driver circuit 10 according to the invention.

In contrast to figure 6, figure 7 illustrates the voltage profile for a large and a small load for a driver circuit 10 which is not provided with a feedback circuit 40, that is to say in which only an approximately $\sin^2$-shaped current is made available, without setting a load-independent edge steepness.

The voltage profile 70 with the respective rise edges 71 and fall edges 72 again corresponds to a large load of 50 pF, while the voltage profile 73 with the corresponding rise edges 74 and fall edges 75 corresponds to a small load of 5 pF.

As can clearly be seen from figure 7, there are large differences in the rise times and fall times of the individual voltage profiles. In the case of the large load of 50 pF, the rise time is approximately 10 ns, while the rise time is only approximately 4 ns in the case of the small load. This means that, in this case, the individual voltage profiles and thus the driver circuit 10 do not exhibit load independence.

Finally, figure 2 illustrates a further embodiment of a driver circuit 10. Identical components to those in the driver circuit 10 in accordance with figure 1 have been provided with identical reference numerals.

The driver circuit 10 again has an input node 11 for an input signal 13 and also an output node 12 for an output signal 14, the output signal 14 being coupled out at the output node 12 and being made available to a

load capacitance. The driver circuit 10 again has a pull-up sub-driver 20 and a pull-down sub-driver 30. The two sub-drivers 20, 30 are connected to the input node 11.

In contrast to figure 1, in the case of the driver circuit 10 in accordance with figure 2, a feedback circuit 40 is provided which has two evaluation circuits 50, 60, in each case one of the evaluation circuits 50, or 60, being connected to a sub-driver 20, or 30, respectively. Each of the evaluation devices 50, 60 is connected to the input node 11, via which the input signal 13 can be coupled in.

Furthermore, a total of two feedback capacitors 41, 42 are provided. Each of these capacitors 41, 42 is arranged in a connecting line leading from the output node 12 to a respective input node 51, 61 of the evaluation devices 50, 60.

The construction of the sub-drivers 20, 30 corresponds to the construction of the sub-drivers from figure 3. Equally, the method of operation of the driver circuit 10 corresponds to the method of operation of the driver circuit according to figures 1 and 3, so that, to avoid repetition, a renewed description is dispensed with and, instead of this, the above explanations are hereby incorporated by reference in their entirety.

New Patent claims

1. A driver circuit, having at least one input node (11) for an input signal and at least one output node (12) for an output signal, having one or more, preferably two, sub-drivers (20, 30) and having a feedback circuit (40), which has one or more evaluation circuits (50, 60) and one or more feedback capacitors (41, 42), the evaluation circuit(s) (50, 60) being connected to the sub-driver(s) (20, 30) and the feedback capacitor(s) (41, 42) respectively being provided between an output node (12) of the driver circuit (10) and an input node (51, 61) of an evaluation circuit (50, 60), the at least one evaluation circuit (50, 60) having a first inverter stage (53, 54), coupled to the input node (51, 61) of the evaluation circuit (50, 60), and also a second inverter stage (56, 57), connected in series with the first inverter stage (53, 54), the first inverter stage (53, 54) being short-circuited with the input node (51, 61).

2. The driver circuit as claimed in claim 1, wherein the at least one input node (11) for the input signal is connected to the at least one sub-driver (20, 30).

3. The driver circuit as claimed in claim 1 or 2, wherein the at least one input node (11) for the input signal is connected to the at least one evaluation circuit (50, 60).

4. The driver circuit as claimed in one of claims 1 to 3, wherein two or more sub-drivers (20, 30) and two or

more evaluation circuits (50, 60) are provided, each sub-driver (20, 30) being connected to an evaluation circuit (50, 60).

5. The driver circuit as claimed in claim 4, wherein two or more feedback capacitors (41, 42) are provided, each feedback capacitor (41, 42) being provided between an output node (12) of the driver circuit (10) and an input node (51, 61) of an evaluation circuit (50, 60).

6. The driver circuit as claimed in one of claims 1 to 5, wherein the input node(s) (51, 61) of the evaluation circuit(s) (50, 60) is/are at low impedance.

7. The driver circuit as claimed in one of claims 1 to 6, wherein the at least one sub-driver (20; 30) has one or more transistors (21, 22, 23; 31, 32, 33).

8. The driver circuit as claimed in one of claims 1 to 7, wherein at least one control transistor (24, 34) is provided in the at least one sub-driver (20, 30), said transistor being respectively connected to an evaluation circuit (50; 60).

9. The driver circuit as claimed in one of claims 1 to 8, wherein the at least one feedback capacitor (41, 42) is designed as a linear capacitor.

10. The driver circuit as claimed in one of claims 1 to 9,
wherein
the at least one feedback capacitor (41, 42) is designed as a nonlinear capacitor.

11. The driver circuit as claimed in claim 10,
wherein
the nonlinear capacitor is formed from at least one PMOS transistor (43) and/or at least one NMOS transistor (44).

12. A method for operating a driver circuit as claimed in one of claims 1 to 11,
wherein
a low-harmonics current is generated in the driver circuit and supplied to a load, and wherein an edge steepness that is independent of the present load situation is set in the driver circuit.

13. The method as claimed in claim 12,
wherein
a $\sin^2$-shaped current is supplied to the load.

14. The method as claimed in claim 12 or 13,
wherein,
in order to set the load-independent edge steepness, the output characteristic of the driver circuit is measured by the feedback circuit and evaluated therein, and wherein the driver strength of the at least one sub-driver is regulated on the basis of the evaluation results.

15. The method as claimed in claim 14,
wherein
the present edge steepness is measured by the at least one feedback capacitor, wherein the measured value is coupled into the at least one evaluation circuit and

evaluated, wherein an output signal is generated in the evaluation circuit, and wherein the output signal controls at least one regulating transistor provided for regulating the driver strength in the at least one sub-driver.

16. The use of a driver circuit as claimed in one of claims 1 to 11 and/or of a method as claimed in one of claims 12 to 15 for improving the electromagnetic compatibility of electronic components, in particular of integrated circuits.

(12) NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT) VERÖFFENTLICHTE INTERNATIONALE ANMELDUNG

(19) Weltorganisation für geistiges Eigentum
Internationales Büro

(43) Internationales Veröffentlichungsdatum
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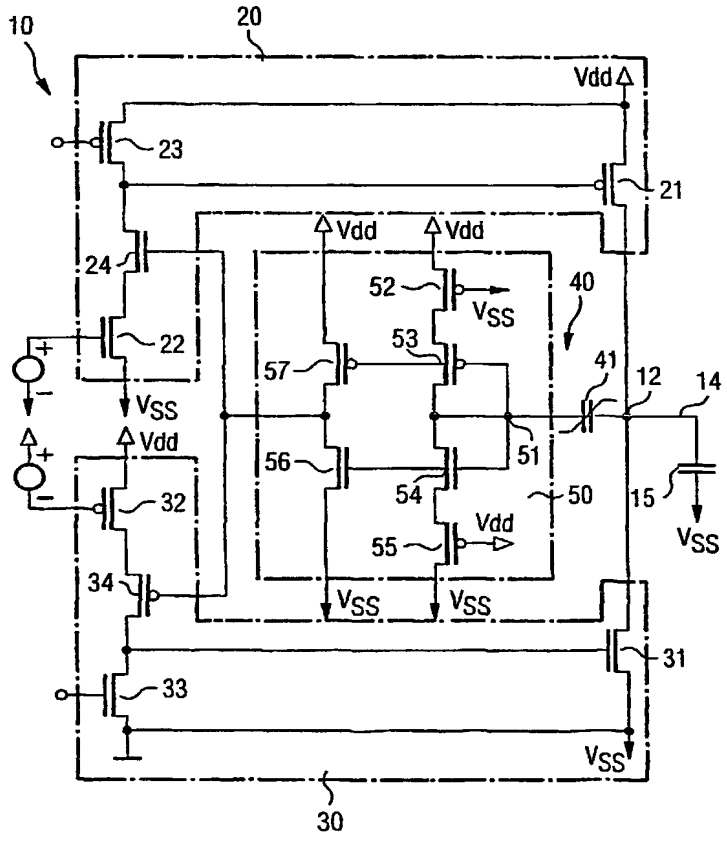
(81) Bestimmungsstaaten *(national)*: CN, JP, KR, US.

[Fortsetzung auf der nächsten Seite]

(54) Title: DRIVER CIRCUIT AND METHOD FOR OPERATING A DRIVER CIRCUIT

(54) Bezeichnung: TREIBERSCHALTUNG UND VERFAHREN ZUM BETREIBEN EINER TREIBERSCHALTUNG



(57) Abstract: The invention relates to a driver circuit (10) for integrated circuits comprising at least one input node (11) for an input signal and at least one output node (12) for an output signal. One or several, preferably two partial drivers (20, 30) supply approximately sine-wave shaped current to the load capacity (15) thereby improving electromagnetic compatibility. A feedback circuit (40) is also provided. Said feedback circuit consists of one or several evaluation circuits (50) and one or several feedback capacitors (41). The evaluation circuits (50) are connected to the partial drivers (20, 30) One feedback capacitor (41, 42) is respectively arranged between an output node (12) of the driver circuit (10) and an input node (51) of an evaluation circuit (50). An evaluation circuit (50) is provided via the feedback condenser (41, 42) between an output node (12) of the driver circuit and an input node (51). The edge steepness of the signal i.e. current which is independent of the actual load, can be produced by means of a feedback circuit (40). The feedback capacitor (41) can, for example, be embodied as a non-linear capacitor.

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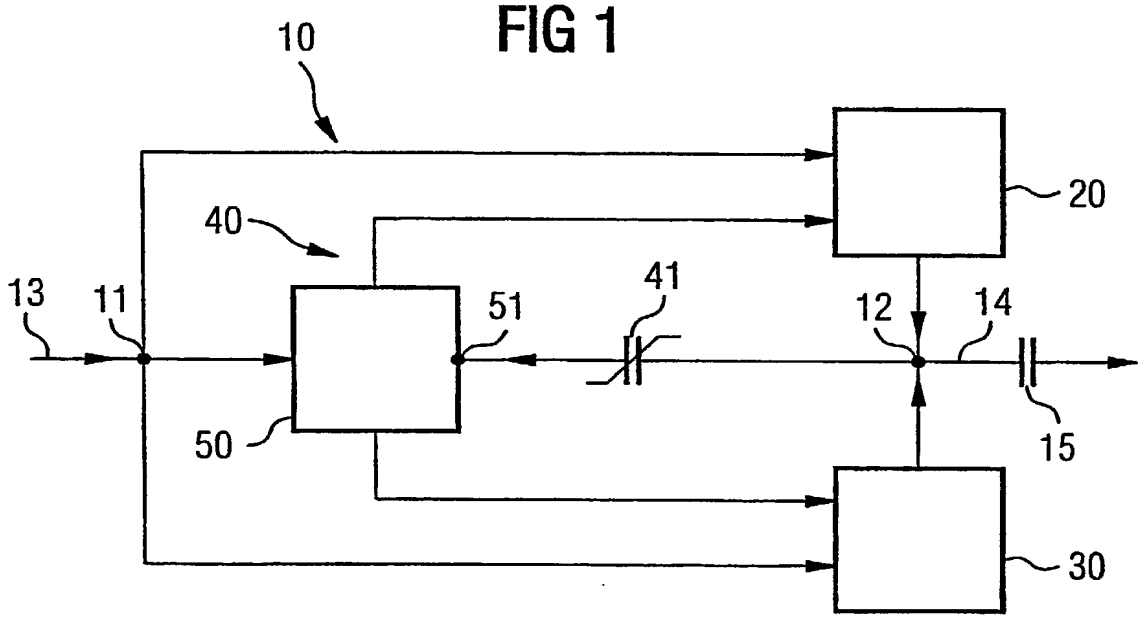
FIG 1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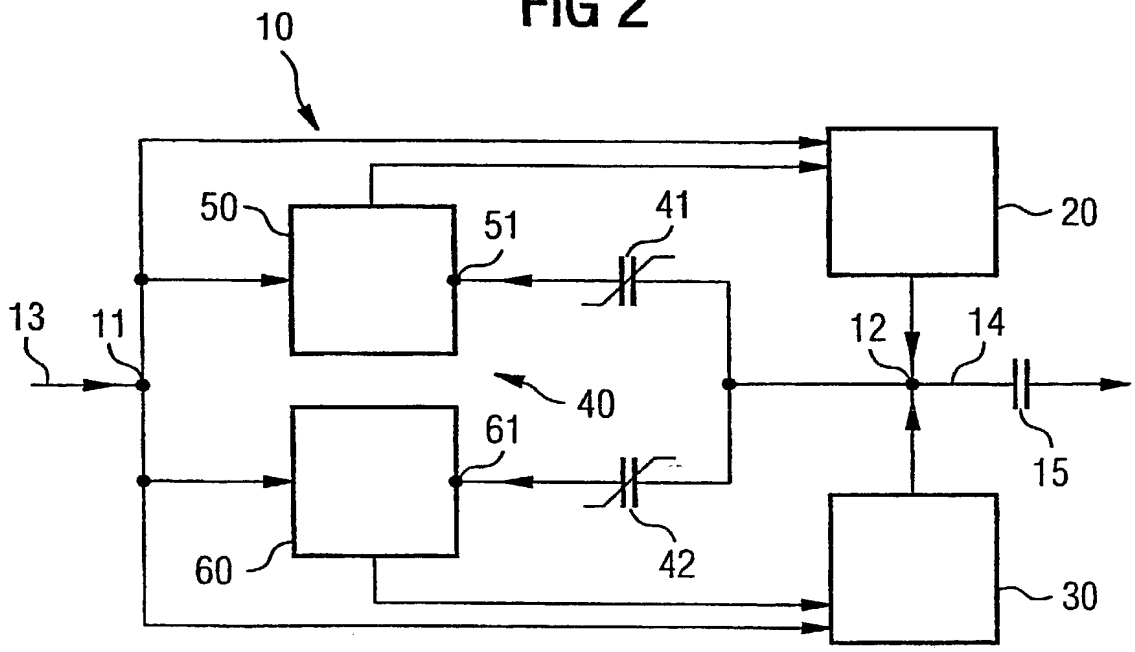
20
40
13
11
51
41
12
14
50
15
30

FIG 2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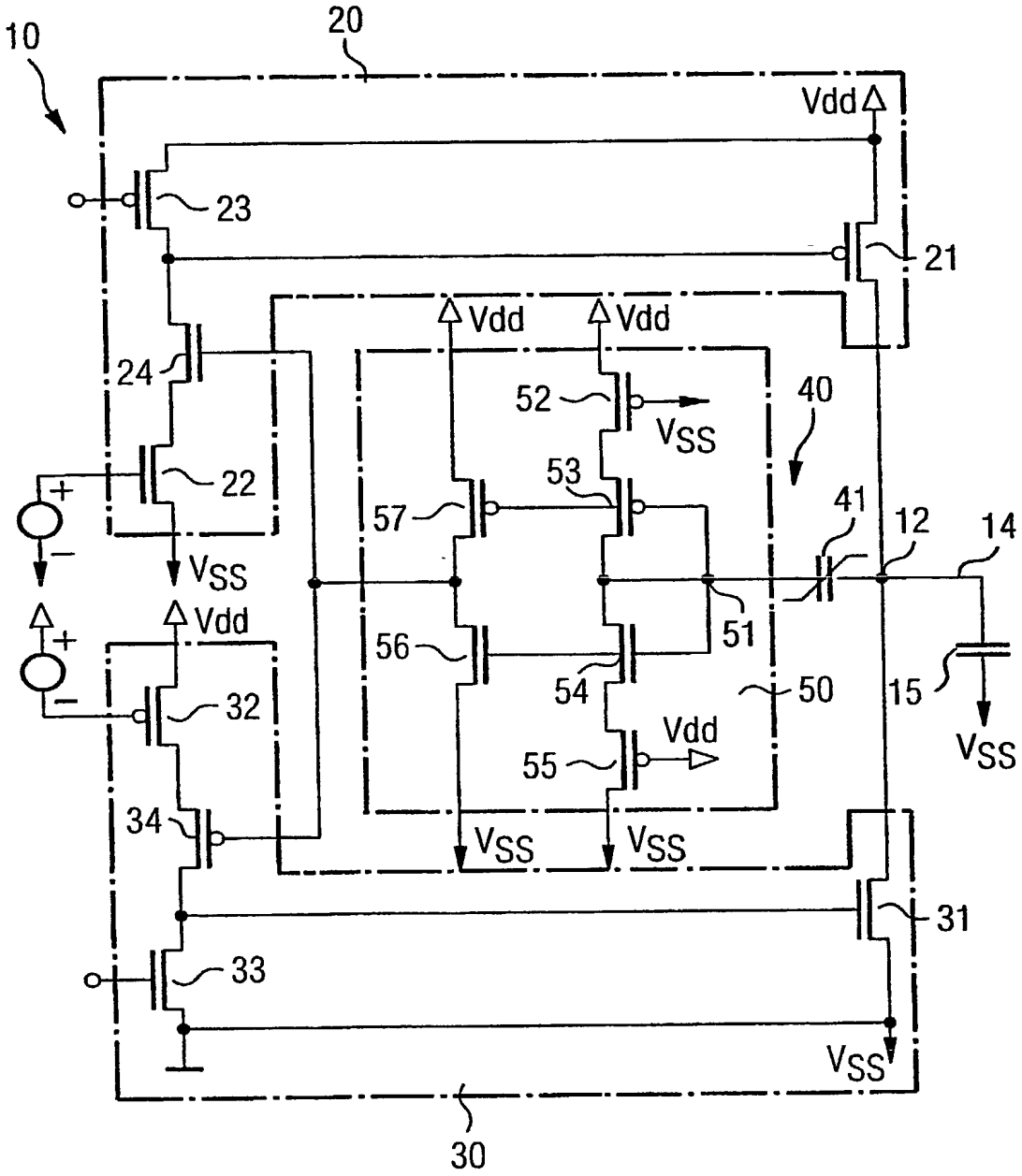
50
51
41
20
13
11
12
14
40
61
15
60
42
30

FIG 3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20
Vdd
23
21
Vdd
Vdd
24
52
40
VSS
22
53
57
41
12
14
VSS
Vdd
56
51
54
50
15
32
Vdd
55
VSS
34
VSS
VSS
31
33
VSS
30

FIG 4

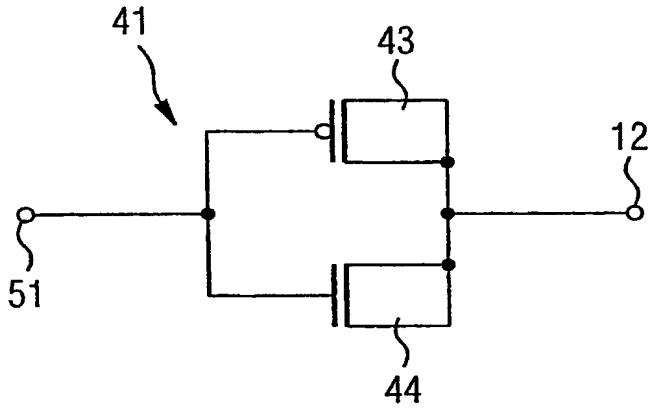


FIG 5

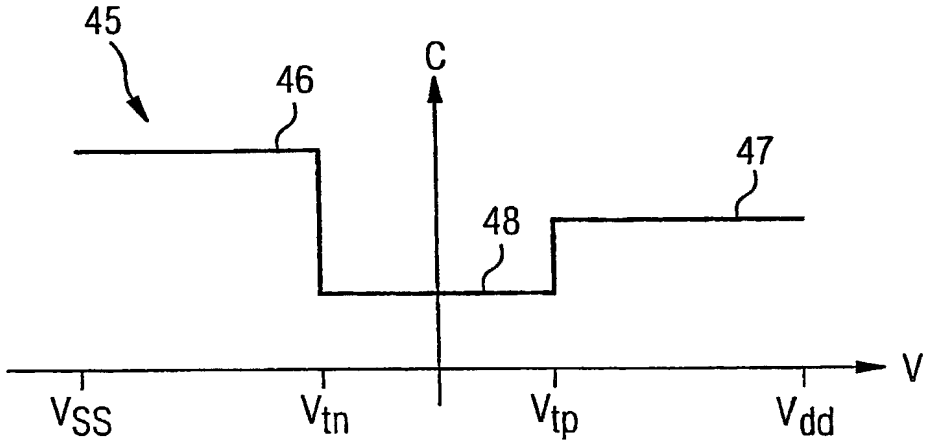
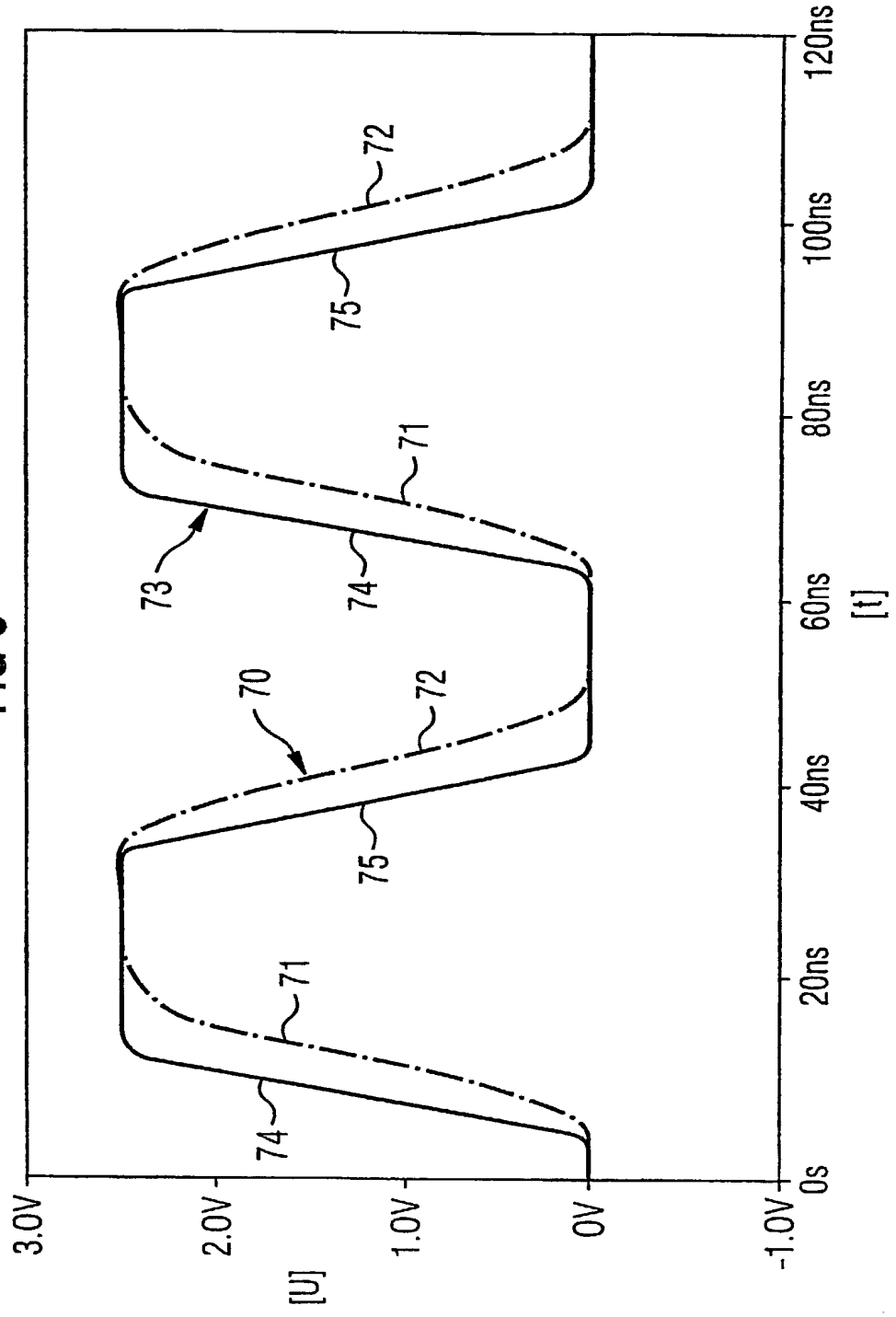


FIG 6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1.0V
0V
-1.0V
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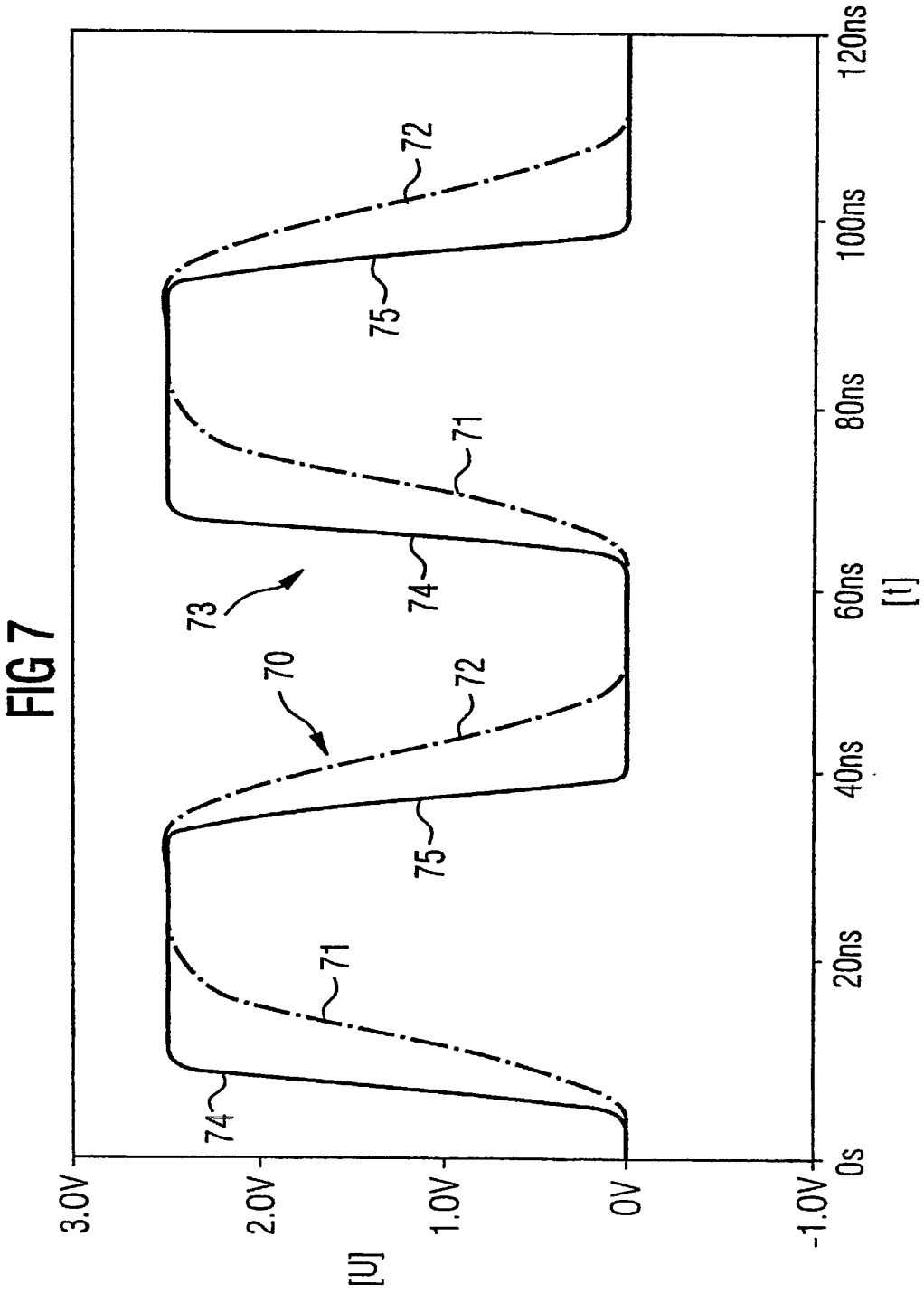
[t]
70
71
72
73
74
75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2.0V
1.0V
0V
-1.0V
[U]
0s
20ns
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80ns
100ns
120ns
[t]
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71
72
73
74
75

FIG 7

#10/069,806

23499 US PCT

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Treiberschaltung und Verfahren zum Betreiben einer Treiberschaltung

_____

the specification of which is attached heretounless the following box is checked:

☒ was filed on February 25, 2002
as United States Application Number or PCT International Application Number 10/069806
_____ and was amended on
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Prior Foreign Applications
(Frühere ausländische Anmeldungen)

		Priority Not Claimed / Priorität nicht beanspruct
19940356.2 (Number) (Nummer)	Germany (Country) (Land)	☐
25 August 1999 (Day/Month/Year Filed) (Tag/Monat/Jahr der Anmeldung)		
____ (Number) (Nummer)	____ (Country) (Land)	☐
____ (Day/Month/Year Filed) (Tag/Monat/Jahr der Anmeldung)		

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____ (Application No.) (Aktenzeichen)	____ (Filing Date) (Anmeldetag)
____ (Application No.) (Aktenzeichen)	____ (Filing Date) (Anmeldetag)

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PCT/DE00/02875 (Application No.) (Aktenzeichen)	23 August 2000 (Filing Date) (Anmeldetag)
____ (Application No.) (Aktenzeichen)	____ (Filing Date) (Anmeldetag)

____ (Status) (patented, pending, abandoned) (Status) (patentiert, schwebend, aufgegeben)	
____ (Status) (patented, pending, abandoned) (Status) (patentiert, schwebend, aufgegeben)	

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Kurt J. Niederluecke - #40,102
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Unterschrift des Erfinders Datum	Inventor's signature Christian Paulus Date 2002-04-11
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Staatsangehörigkeit	Citizenship Germany
Postanschrift	Post Office Address
Vor- und Zuname des zweiten Miterfinders (falls zutreffend)	Full name of second joint inventor, if any Ralf Klein
Unterschrift des zweiten Erfinder Datum	Second Inventor's signature Ralf Klein Date 2002-04-15
Wohnsitz	Residence Walhalla-Str. 20, 80639 Munchen, Deutschland
Staatsangehörigkeit	Citizenship Germany DEX
Postanschrift	Post Office Address

100 X 200

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(Supply similar information and signature for third and subsequent joint inventors.)

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